UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte LOUIS M. MELI

Appeal No. 2006-1558
Application No. 09/313,037

ON BRIEF

Before HAIRSTON, SAADAT, and HOMERE, Administrative Patent Judges.

HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1 through 10.

The disclosed invention relates to a data processing device that stores at least two addresses in parallel in a register circuit.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A data processing device, comprising [sic, :]

a register circuit for storing at least two addresses in parallel;

an address selector arranged to cycle through a set of states in which respective ones of the at least two addresses become a currently selected address respectively;

an instruction execution unit having an instruction set that contains a memory access instruction, execution of the memory access instruction causing the instruction execution unit to issue memory access signals with an access address determined from the currently selected address, execution of the memory access instruction further causing the address selector to cycle to a next one of the states; and

a control register that is instruction-settable to respective control states that control whether or not the processing device updates the at least two addresses as a side-effect of executing the memory access instruction.

The references relied on by the examiner are:

Pawloski 5,426,769 June 20, 1995

Dallas Semiconductor, Product Review DS87C550, Sept. 16, 1998, pages 1 through 47.

Claims 1 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Pawloski in view of the Dallas Semiconductor Product Review (hereinafter Dallas Semiconductor).

Reference is made to the final rejection, the brief and the answer for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1 through 10.

According to the examiner's findings (final rejection, pages 2 and 3), Pawloski discloses all of the data processing device limitations of claim 1 except for: "a register circuit for storing at

least two addresses in parallel; an address selector arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively; or the execution of the memory access instruction further causing the address selector to cycle to a next one of the states." The examiner is of the opinion (final rejection, page 3) that Dallas Semiconductor discloses the following: "a register circuit for storing at least two addresses in parallel in Figure 1 elements DPTR0 and DPTR1, an address selector (data pointer select bit SEL page 13 4th paragraph) arranged to cycle a set of states in which respective ones of the at least two addresses become a currently selected address respectively at page 14, first paragraph, and execution of the memory access instruction further causing the address selector to cycle to a next one of the states at page 14 first paragraph and table of assembly code." Since Pawloski and Dallas Semiconductor both relate to 8051 microcontrolller technology, and "Dallas Semiconductor states that the incorporation of two data pointer registers improves the efficiency of data moves," the examiner concluded "it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate Dallas's shadow DPTR register in Palowski [sic, Pawloski]" (final rejection, page 4).

Appellant argues (brief, page 4) :

> [A]s clearly described in Dallas on page 14, DPRTO [sic, DPTR0] and DPTR1 consist of non-parallel registers located within an integrated circuit chip. Namely, Dallas states that "DPTR1 is located at the next two register locations (up from DPTR0)." Accordingly, Dallas fails to disclose "a register circuit for storing at least two addresses in *parallel*."

In response, the examiner states (answer, page 11) that Dallas Semiconductor describes "a register circuit for storing at least two addresses in parallel" because:

> "Parallel" within the context of VLSI design would indicate that the two registers are geographically located next to each other. Principles of VLSI design place two adjacent registers in a register file parallel to each other on the silicon. Dallas' disclosure that DPTR0 and DPTR1 are located in two adjacent locations within the register file indicates that the two registers are parallel on the silicon die.

The examiner's contentions to the contrary, notwithstanding the record on appeal, is silent as to the geographical placement of registers in a VLSI design. The mere speculation of the examiner as to the specific geographical placement of registers in a VLSI design cannot serve as the basis of a finding of obviousness. In an obviousness determination, only the objective teachings of the prior art or knowledge generally available to one of ordinary skill in the art can be used by the examiner. See In re Lee, 277 F.3d 1338, 1344, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002). Dallas merely states (page 14, column 1) that the register "DPTR1 is located at the next two register locations (up from DPTR0)." The Dallas Semiconductor 8051 microcontroller diagram (Figure 1, page 3) shows the registers connected together, but the remainder of the publication is silent as to a parallel connection that enables "storing at least two addresses in parallel." Thus, the obviousness rejection of claims 1 through 10 is reversed because a prima facie showing of obviousness cannot be built on speculation by the examiner.

DECISION

The decision of the examiner rejecting claims 1 through 10 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON)
Administrative Patent Judge)
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)
MAHSHID D. SAADAT) BOARD OF PATENT
Administrative Patent Judge)
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